PTO/SB/21 (01-08)

OIPE IAP18 FEB 15 2008 PATENT & TRADEMARK OFFICE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/773,522
Filing Date	February 6, 2004
First Named Inventor	Huang, Herb H.
Art Unit	2815
Examiner Name	Matthew C. Landau
Attorney Docket Number	021653-000900US

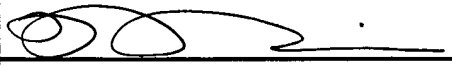
ENCLOSURES *(Check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please identify below):

Return Postcard

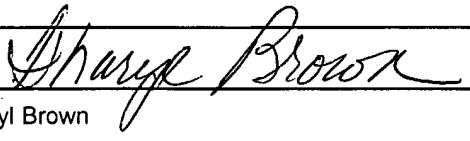
Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	Kent J. Tobin		
Date	February 12, 2008	Reg. No.	39,496

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature			
Typed or printed name	Sharyl Brown	Date	February 12, 2008

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2007

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 510

Complete if Known	
Application Number	10/773,522
Filing Date	February 6, 2004
First Named Inventor	Huang, Herb H.
Examiner Name	Matthew C. Landau
Art Unit	2815
Attorney Docket No.	021653-000900US

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 20-1430 Deposit Account Name: Townsend and Townsend and Crew LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	310	155	510	255	210	105	
Design	210	105	100	50	130	65	
Plant	210	105	310	155	160	80	
Reissue	310	155	510	255	620	310	
Provisional	210	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	210	105
Multiple dependent claims	370	185

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____	-20 or HP = _____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____	-3 or HP = _____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims: Fee ($) _____ Fee Paid ($) _____

3. APPLICATION SIZE FEE

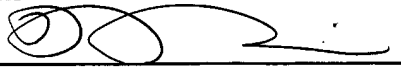
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round **up** to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Filing a brief in support of an appeal	510

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 39,496	Telephone 650-326-2400
Name (Print/Type)	Kent J. Tobin		Date February 12, 2008

61282604 v1

PATENT
Attorney Docket No. 021653-000900US
Client Ref. No.: I-02-049

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Herb H. Huang et al. Application No.: 10/773,522 Filed: February 6, 2004 For: SEMICONDUCTOR MEMORY CELL WITH BURIED DOPANT BIT LINES AND SALICIDED POLYSILICON WORD LINES ISOLATED BY AN ARRAY OF BLOCKS Customer No.: 20350	Confirmation No. 6545 Examiner: Matthew C. Landau Technology Center/Art Unit: 2815 APPELLANTS' BRIEF UNDER 37 CFR §41.37

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Final Office Action mailed September 13, 2007, and further to the Notice of Appeal filed December 13, 2007, Appellants submit this Brief on Appeal.

1. REAL PARTY IN INTEREST

The real party in interest for the above-identified application is the Semiconductor Manufacturing International Corporation ("SMIC"), having its principal place of business at 18 Zhang Jiang Rd. Pudong New Area, Shanghai 201203, China. Assignment of the instant patent

application to SMIC was recorded in the U.S. Patent and Trademark Office on February 6, 2004 at Reel 014970/Frame 0069.

2. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the present appeal.

3. STATUS OF CLAIMS

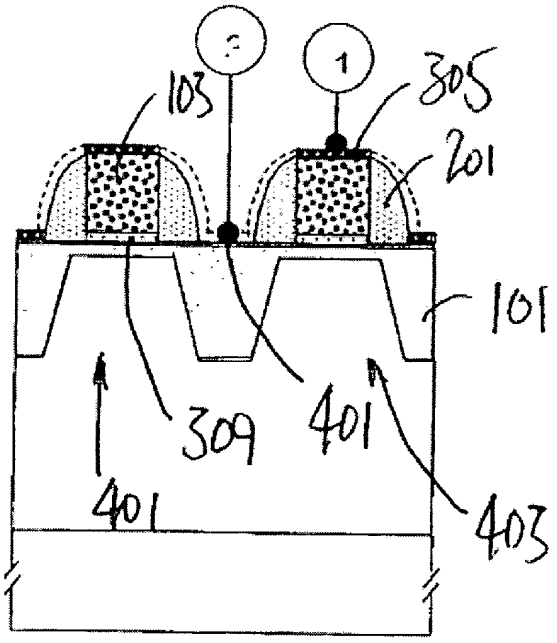
Claims 1-10 are pending and subject to this appeal. Claims 1-10 were rejected under 35 U.S.C. § 103(a) based on the grounds set forth in the Final Office Action mailed on September 13, 2007.

4. STATUS OF AMENDMENTS

All amendments to the claims have been entered. In accordance with 37 C.F.R. § 1.192(c)(9), a copy of the claims involved in the appeal are contained in the attached Appendix.

5. SUMMARY OF CLAIMED SUBJECT MATTER

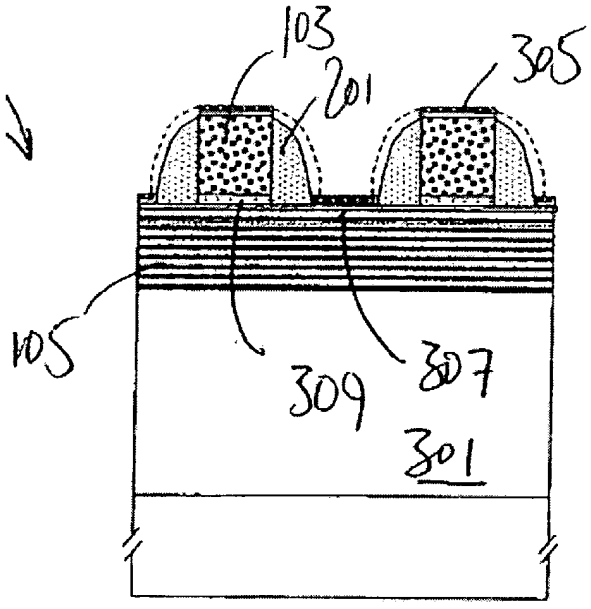
Embodiments of the present invention relate to manufacturing of semiconductor devices. As shown in the cross-sectional view of Figure 4 (reproduced in part below), one feature of the claimed embodiments is formation of a trench isolation structure (101), and application of a refractory metal layer (305) over an exposed portion of that trench isolation structure (101), such that refractory metal over the trench is separated from an adjacent gate by a gate spacer (201).



Accordingly, claim 1 recites as follows

> 1. A method for manufacturing ROM memory devices, the method comprising:
>
> . . . forming a first sidewall spacer overlying a first side of the gate structure and a second sidewall spacer overlying a second side of the gate structure, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being configured to extend over and overlap a portion of the trench isolation structure and to extend over and overlap a portion of source/drain regions, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being adapted to separate the gate structure from the trench isolation region and to separate the gate structure from the source/drain regions . . . . (Emphasis added)

Another aspect of embodiments of the present invention shown in the cross-sectional view of Figure 3 (reproduced in part below), is the formation of silicided regions (305 and 307) overlying the gate structure and the source/drain regions, respectively.



Independent claim 1 thus also recites formation of such silicided regions:

> 1. A method for manufacturing ROM memory devices, the method comprising:
>
> . . . applying a refractory metal layer overlying the gate structure including the first side wall spacer and the second sidewall spacer and exposed portion of the trench isolation structure;

alloying the refractory metal layer to the gate structure and exposed portions of source/drain regions to form silicided regions overlying the gate structure and source/drain regions; and

selectively removing the refractory metal layer from the sidewall spacers and exposed portion of the trench isolation structure. (Emphasis added)

Still another feature of the claimed embodiments shown in Figure 3 above, is the continuous extension of the bit line portion (105) underneath the gate structure (103). Accordingly, independent claim 1 indicates such continuous bit lines:

1. A method for manufacturing ROM memory devices, the method comprising:

forming a trench isolation structure within a cell region of a semiconductor substrate, the cell region being in an array region for ROM memory devices, the trench isolation structure being provided to separate a continuous bit line region of the cell from another continuous bit line region from another cell . . . . (Emphasis added)

This appeal brief includes the following table providing a mapping of the elements of the independent claim to the relevant page and line numbers in the specification.

Claim 1	**Specification**
1. forming a trench isolation structure within a cell region of a semiconductor substrate, the cell region being in an array region for ROM memory devices, the trench isolation structure being provided to separate a continuous bit line region of the cell from another continuous bit line region from another cell;	Page 3, line 18-page 3, line 23 Page 8, line 15-page 3, line 17
forming a gate structure within the cell region;	Page 3, lines 20-21 Page 8, lines 14 Page 9, line 3
forming a first sidewall spacer overlying a first side of the gate structure and a second sidewall spacer overlying a second side of the gate structure, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being configured to extend over and overlap a portion of the trench isolation structure and to extend over and overlap a portion of source/drain regions, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being adapted to separate the gate structure from the trench isolation region and to separate the gate structure from the source/drain regions;	Page 3, line 21-page 4, line 8

applying a refractory metal layer overlying the gate structure including the first side wall spacer and the second sidewall spacer and exposed portion of the trench isolation structure;	Page 3, lines 23-25 Page 8, lines 18-19 Page 9, lines 9-10
alloying the refractory metal layer to the gate structure and exposed portions of source/drain regions to form silicided regions overlying the gate structure and source/drain regions; and	Page 3, lines 25-28 Page 8, lines 20-22 Page 9, lines 12-14
selectively removing the refractory metal layer from the sidewall spacers and exposed portion of the trench isolation structure.	Page 3, lines 27-28 Page 8, lines 23-24 Page 9, lines 15-17

The dependent claims describe the structure of the ROM memory in addition to that recited in the independent claims. For example, dependent claim 2 recites that the refractory metal layer is titanium or cobalt; dependent claims 3,4, and 8 describe the structure of the trench isolation region; and claims 5 and 9 recite that the memory cell has a channel region using a length of about 0.25 micron and less, and that the gate structure has a width of 0.25 micron and less respectively. Dependent claim 6 recites that the first sidewall spacer and the second sidewall spacer comprise of a dielectric material. Other dependent claim 7 recites that the buried bit line structure is within the source/drain regions. Still other dependent claim 10 recites that the array has at least eight cells by eight cells. Support for these dependent claims may be found in the specification at least at **¶[0010]** - **¶[0012]** and at **¶[0021]** - **¶[0023]**.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-4, and 6-8 stand rejected under 35 U.S.C. §103(a) as over U.S. Patent 6,372,580 to Shiau ("the Shiau Patent") in view of U.S. Patent 6,847,087 to Yang et al. ("the Yang Patent").

B. Claims 5 and 9 stand rejected under 35 U.S.C. §103(a) as obvious over the Shiau Patent with the Yang Patent and further in view of U.S. Patent Publication No. 2004/0262650 to Iwata et al. ("the Iwata Publication").

C. Claim 10 stands rejected under 35 U.S.C. §103(a) as obvious over the Shiau Patent with the Yang Patent and further in view of U.S. Patent 5,506,160 to Chang ("the Chang Patent").

7. ARGUMENT

A. Rejection of Claims as obvious over the Shiau Patent in view of the Yang Patent

The Shiau Patent is the primary reference relied upon by the Examiner. Like the instant application, the Shiau Patent is directed to a method for manufacturing a semiconductor device and discloses formation of a thin refractory metal (See col. 4, lines 57-58).

Unlike the instant application however, the Shiau Patent does not even contemplate the use of a trench isolation structure. Specifically, as conceded by the by Examiner in the latest Office Action, the Shiau Patent fails to teach formation of a trench isolation structure within a cell or the arrangement of the isolation structure (See Office Action Mailed June 4, 2007, page 4, lines 1-2).

In an effort to provide the teaching lacking from the Shiau Patent, the Examiner has combined that reference with the Yang Patent. However, the Examiner is respectfully reminded that in order to establish a prima facie case of obviousness, there must be some suggestion in either the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Such teaching or suggestion to make the claimed combination must be found in the prior art, not in applicant's own disclosure. In re Vaeck, 947 F.2d 488 (Fed.Cir. 1991).

Here, there is no suggestion in the Shiau Patent that would motivate one of ordinary skill in the art to combine it with the Yang Patent. Specifically, an object of the Shiau Patent is the development of a silicide layer to reduce the electrical resistance in the word and bit lines.

> Since the silicide layer is deposited in a single step, it can be easily incorporated into the manufacturing process. Furthermore, the suicide (silicide) layer reduces electrical resistance in both the word lines and bit lines resulting in improved operating speeds of the memory cells. (Emphasis added; col. 5, lines 17-21)

By contrast, as shown in Figure 2(a) (reproduced below) of the Yang Patent, this reference utilizes a contact plug (102) which penetrates the surface of the drain region and buried bit lines in order to short-circuit the drain and bit lines:

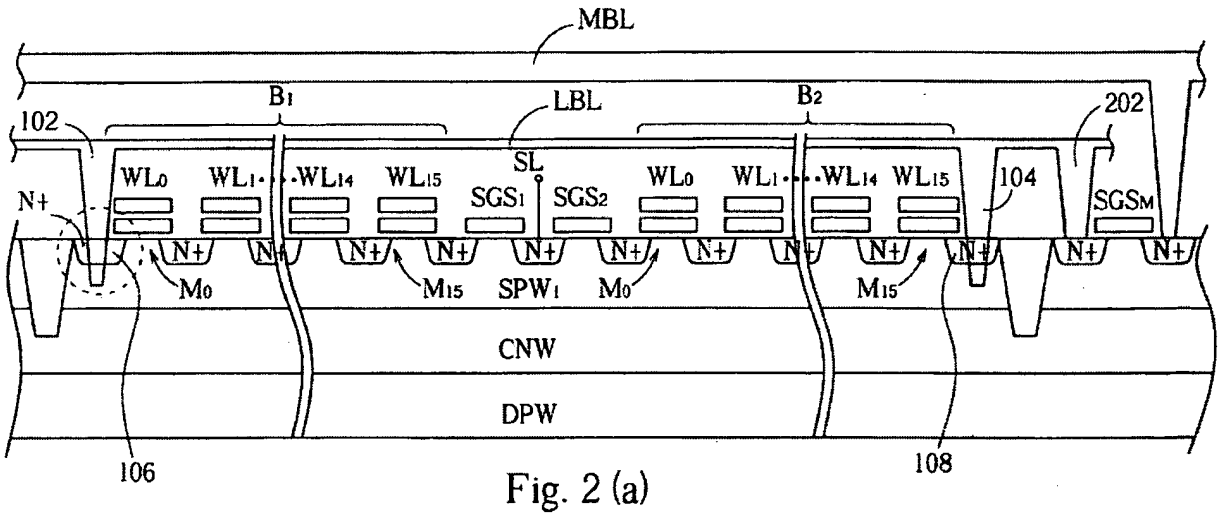


Fig. 2 (a)

contact plug **102** is electrically connected with a drain **106** of the NMOS memory transistor M_0 of the NAND cell block B_1. As specifically indicated in the circle regions of FIG 2(a), the contact plug **102** penetrates a junction of the drain **106** and the underlying buried bit line SPW_1, thereby short-circuiting the drain **106** and the subjacent buried bit line SPW_1. (Emphasis added, col. 5, lines 11-15)

Accordingly, use of the salicide process and the formation of a silicide layer as taught in the Shiau Patent, in combination with the Yang Patent, would be nonsensical. Specifically, the silicide layer of the Shiau Patent is used to decrease electrical resistance of the drain and bit line region, while the contact plug of the Yang Patent is electrically coupled to short-circuit this region. In view of this conflicting function, use of the contact plug of the Yang Patent is plainly inconsistent with the expressed objective of the Shiau Patent.

Based at least upon this key difference between the Shiau and Yang Patents, one of ordinary skill in the art would hardly have been motivated to combine these references to arrive at the claimed invention.

Of course, the instant application contains substantial disclosure regarding formation of a trench isolation structure and application of a refractory metal layer over an exposed portion of the trench isolation structure. However, the Examiner is respectfully reminded that any suggestion to combine references must be found in the prior art, and not be based upon applicants' own disclosure:

> The tendency to resort to "hindsight" based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However,

> impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. (Emphasis added; MPEP 2142)

In view of the failure of the Shiau and Yang Patents to provide any reasonable motivation for their combination, it is respectfully asserted that the pending claims cannot be considered obvious in light of these references.

Independent claim 1 is patentable over the cited references for at least the reasons under 35 U.S.C. §103(a). Additionally, claims 2-10 which depend upon claim 1 should also be patentable based on the same rationale as discussed for claim 1.

B. Rejection of Claims as obvious over the Shiau and Yang Patents Further in Combination with the Iwata Publication

As discussed extensively above, the Shiau and Yang Patents, taken even in combination, fail to teach or suggest all of the elements of the pending claims. This missing teaching is not cured by consideration of the Iwata Publication. Specifically, Iwata Publication does not appear to disclose continuous extension of the bit line portion underneath a gate structure in the manner of the claimed embodiments.

C. Rejection of Claims as obvious over the Shiau and Yang Patents Further in Combination with the Chang Patent

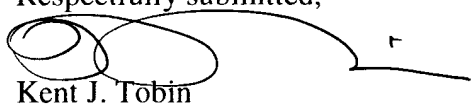
As discussed extensively above, the Shiau and Yang Patents, taken even in combination, fail to teach or suggest all of the elements of the pending claims. This missing teaching is not cured by consideration of the Chang Patent. Specifically, Chang Patent does not appear to disclose the formation of sidewall spacers separating a gate from trench isolation structures.

Based upon the absence of any motivation or suggestion regarding all of the claim elements in any of the reference combinations relied upon by the Examiner, it is respectfully asserted that the claims cannot legitimately be viewed as obvious. Continued maintenance of the obviousness claim rejections is improper, and the application should now be passed to issuance.

8. CONCLUSION

For the reasons set forth above, it is respectfully submitted that the obviousness claim rejections should be reversed.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400;
Fax: 650-326-2422

61265620 v1

9. CLAIMS APPENDIX

1. A method for manufacturing ROM memory devices, the method comprising:

forming a trench isolation structure within a cell region of a semiconductor substrate, the cell region being in an array region for ROM memory devices, the trench isolation structure being provided to separate a continuous bit line region of the cell from another continuous bit line region from another cell;

forming a gate structure within the cell region;

forming a first sidewall spacer overlying a first side of the gate structure and a second sidewall spacer overlying a second side of the gate structure, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being configured to extend over and overlap a portion of the trench isolation structure and to extend over and overlap a portion of source/drain regions, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being adapted to separate the gate structure from the trench isolation region and to separate the gate structure from the source/drain regions;

applying a refractory metal layer overlying the gate structure including the first side wall spacer and the second sidewall spacer and exposed portion of the trench isolation structure;

alloying the refractory metal layer to the gate structure and exposed portions of source/drain regions to form silicided regions overlying the gate structure and source/drain regions; and

selectively removing the refractory metal layer from the sidewall spacers and exposed portion of the trench isolation structure.

2. The method of claim 1 wherein the refractory metal layer is titanium or cobalt.

3. The method of claim 1 wherein the trench isolation region is an STI region.

4. The method of claim 3 wherein the STI region comprises silicon dioxide.

5. The method of claim 1 wherein the memory cell has a channel region using a length of about 0.25 micron and less.

6. The method of claim 1 wherein the first sidewall spacer and the second sidewall spacer comprise of a dielectric material.

7. The method of claim 1 wherein the buried bit line structure is within the source/drain regions.

8. The method of claim 1 wherein the trench isolation is within the semiconductor substrate at a predetermined depth, the predetermined depth being greater than a junction depth of the buried bit line.

9. The method of claim 1 wherein the gate structure has a width of 0.25 micron and less.

10. The method of claim 1 wherein the array has at least eight cells by eight cells.

11-26. (Canceled)

10. EVIDENCE APPENDIX

None

11. RELATED PROCEEDINGS APPENDIX

None